REMARKS

The Official Action dated July 7, 2006 has been received and its contents noted. The Examiner is thanked for reviewing this application and for indicating the allowance of claims 2-5.

As previously, claims 1-5 are presently pending in the instant application, of which claim 1 is independent.

Claim 1 stands rejected under 35 U.S.C. §103(a) as unpatentable over Iwata et al. (U.S. Patent No. 4,514,826 – hereafter Iwata) in view of Ibaraki et al. (U.S. Patent No. 5,617,476 – hereafter Ibaraki, previously applied). This rejection is respectfully traversed at least for the reasons provided below.

As submitted previously, the present invention as set forth in independent claim 1, is directed to an image processing apparatus including at least two signal processor modules interconnected with each other in series, each of these signal processor modules having an input port through which data is input, a memory which stores data, a signal processor portion which carries out processing on input data according to a program and an output port through which data is output, wherein at least one of the signal processor modules outputs in parallel both unprocessed input data and processed data obtained by processing the input data.

Iwata, on the other hand, discloses a relational algebra engine which performs a set of operations at high speed in a database system dealing with a relational model. In the rejection, the Examiner alleged that Iwata discloses an image processing apparatus comprising at least two signal processor modules (PE1, PE2 in Fig. 3) interconnected in series. However, Applicants respectfully assert that there is no teaching, disclosure or suggestion of any image processing apparatus or capability in the relational algebra engine for using in a relational database system of Iwata.

Further, PE1 and PE2 of Iwata are processing engines in a sort engine SE, according to col. 2, lines 59-64, for example, of Iwata. It is clearly disclosed that Fig. 3 of Iwata is a block diagram of a relational algebra engine for performing sort/merge algorithm, which is clearly and completely unrelated to imaging processing and the signal processor modules utilized in image processing in Applicants' claimed invention. Should the Examiner

continues asserting that Iwata teaches an image processing system and signal processors, Applicants would respectfully request the Examiner to provide support by pointing out where in Iwata such disclosure can be found.

Still further, the Examiner stated, "Iwata does not specifically states that at least one of signal processor modules outputs in parallel both unprocessed input data and processed data obtained by processing the input data." To cure the deficiency of Iwata, the Examiner cited Ibaraki.

In response to the application of Ibaraki as a secondary reference as teaching a separator 81 in fig. 8A that outputs both processed data and unprocessed data in parallel, Applicants respectfully direct the Examiner's attention to Applicants' remarks submitted in the previously submitted Amendment filed April 27, 2006.

As previously submitted, Ibaraki discloses an encryption device 223' in Fig. 8A having a separator 81 that receives sample data and separates the data into unprocessed portions and processed portion based on a processing flag information and masking signal provided to the separator. The portions of the data to be processed are transmitted to block encryption device 82 and eventually to synthesizer 83. The unprocessed portions (i.e., portions not to be encrypted) that have been separated from the processed portions (i.e., portions to be encrypted) are fed into the synthesizer 83 without being encrypted. For detailed description of Fig. 8A, the Examiner is invited to review col. 12, lines 28-41 of Ibaraki, which is shown below for Examiner's convenience:

> FIG. 8A is a block diagram of an encryption device 223' which is a modification of that shown in FIG. 3, and applies block encryption. As shown in FIG. 8A, this encryption device 223 comprises a separator 81, block encryption device 82, and synthesizer 83. The audio signal, process flag, and masking signal are input to the separator 81, which outputs as processed data the data of the position where the masking signal is `1` when the process flag of the sample data is `1`, and outputs the remaining data as unprocessed data. The block encryption device 82 then encrypts and outputs the processed data. The synthesizer 83 then synthesizes the unprocessed data and the output from the block encryption device 82; this operation is controlled by inputting the process flag and the masking signal to the synthesizer 83 to inverse the operation of the separator 81.

Clearly, Ibaraki does not teach, disclose or suggest least one of the signal processor modules outputs in parallel both unprocessed input data and processed data obtained by processing the input data, as recited in Applicants' claim 1. Rather, Ibaraki takes input data and divides the data into unprocessed portions and processed portions based on flag and masking information provided to the separator 81.

Moreover, the Examiner erroneously equated the separator 81 to Applicants' signal processor modules. As disclosed by Ibaraki and as explained above, the separator 81 is merely a data separator that separates sample data so that portions that are flagged are encrypted by the block encryption device 82. Applicants respectfully reiterate that the separator 81 of Ibaraki is not a signal processor module and does not have its own memory and signal processor portion.

The requirements for establishing a *prima facie* case of obviousness, as detailed in MPEP § 2143 - 2143.03 (pages 2100-122 - 2100-136), are: first, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference to combine the teachings; second, there must be a reasonable expectation of success; and, finally, the prior art reference (or references when combined) must teach or suggest all of the claim limitations. As Iwata is deficient in teaching, disclosing an image processing apparatus comprising at least two signal processor modules wherein at least one of the signal processor modules output in parallel both unprocessed input data and processed data obtained by processing the input data, and as Ibaraki fails to teach, disclose or suggest, among other features, at least one of the signal processor modules output in parallel both unprocessed input data and processed data obtained by processing the input data, the combination of Iwata and Ibaraki is improper, and a *prima facie* case of obviousness has not been established. Should the Examiner maintains the rejection based on the combination of Iwata and Ibaraki, Applicants would respectfully request the Examiner to at least provide the rationale for combining a relational algebra engine for use in a relational database of Iwata with an audio scrambling system of Ibaraki, in addition to their deficiencies noted above.

Therefore, in view of the foregoing, it is respectfully requested that the rejection of claim 1 be reconsidered and withdrawn by the Examiner, that all claims 1-5 be allowed and that the application be passed to issue. Should the Examiner believe a conference would be of benefit in expediting the prosecution of the instant application he is hereby invited to telephone counsel to arrange such a conference.

Respectfully submitted,

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